

What is claimed is:

1. A method comprising:

storing in memory a queue descriptor including a head
pointer pointing to a first element in a queue and a tail

5 pointer pointing to a last element in the queue;

in response to a command to perform an enqueue or
dequeue operation with respect to the queue, fetching from
the memory to a cache one of either the head pointer or tail
pointer; and

10 returning to the memory from the cache portions of the
queue descriptor modified by the operation.

2. The method of claim 1 including fetching the head
pointer and not the tail pointer in response to a command to
15 perform a dequeue operation.

3. The method of claim 1 including fetching the tail
pointer and not the head pointer in response to a command to
perform an enqueue operation.

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4. The method of claim 1 including returning to memory the
head pointer and not the tail pointer if only dequeue
operations were performed on the queue.

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10. The method of claim 9 including setting the first valid bit if a dequeue operation is performed with respect to the queue descriptor, or an enqueue operation is performed with respect to the queue descriptor while the queue is empty.

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11. The method of claim 9 including setting the second valid bit if an enqueue operation is performed with respect to the queue descriptor.

10 12. The method of claim 9 including setting a pointer's valid bit when the pointer is fetched from the memory to the cache.

13. The method of claim 9 including returning to the memory pointers whose valid bits have been set.
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14. An apparatus comprising:

memory for storing queue descriptors which include a head pointer pointing to a first element in a queue and a tail pointer pointing to a last element in the queue;
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a cache for storing queue descriptors corresponding to up to a number of the memory's queue descriptors; and

a processor configured to:

fetch from the memory to the cache one of either
25 the head pointer or the tail pointer of a particular queue

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descriptor in response to a command to perform an enqueue or a dequeue operation with respect to the particular queue descriptor; and

return to the memory from the cache portions of
5 the queue descriptor modified by the operation.

15. The apparatus of claim 14 wherein the processor is configured to fetch the head pointer and not the tail pointer in response to a command to perform a dequeue
10 operation.

16. The apparatus of claim 14 wherein the processor is configured to fetch the tail pointer and not the head pointer in response to a command to perform an enqueue
15 operation.

17. The apparatus of claim 14 wherein the processor is configured to return to the memory the head pointer and not the tail pointer when only dequeue operations were performed
20 on the queue.

18. The apparatus of claim 14 wherein the processor is configured to return to the memory the tail pointer and not the head pointer if only enqueue operations were performed
25 on the queue while the queue was unempty.

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23. The apparatus of claim 21 wherein the processor is configured to set the second valid bit if an enqueue operation is performed with respect to the queue descriptor.

5 24. The apparatus of claim 21 wherein the processor is configured to set a pointer's valid bit when the pointer is fetched from the memory to the cache.

25. The apparatus of claim 21 wherein the processor is
10 configured to return to the memory the pointers whose valid bits has been set.

26. An article comprising a computer-readable medium that stores computer-executable instructions for causing a
15 computer system to:

store in memory a queue descriptor including a head pointer pointing to a first element in a queue and a tail pointer pointing to a last element in the queue;

in response to a command to perform an enqueue or
20 dequeue operation with respect to a queue, fetch from memory to a cache one of either a head pointer pointing to a first element in a queue or a tail pointer pointing to a last element in the queue; and

return to the memory from the cache the portions of the
25 queue descriptor modified by the operation.

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27. The article of claim 26 including instructions to cause the computer system to:

fetch the head pointer and not the tail pointer in
5 response to a command to perform a dequeue operation; or

fetch the tail pointer and not the head pointer in
response to a command to perform an enqueue operation.

28. The article of claim 26 including instructions to cause
10 the computer system to return to memory:

the head pointer and not the tail pointer if only
dequeue operations are performed on the queue;

the tail pointer and not the head pointer if only
enqueue operations are performed on the queue while the
15 queue is unempty; or

both the head pointer and tail pointer if both an
enqueue and a dequeue are performed on the queue, or an
enqueue operation was performed on the queue while the queue
is empty.

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29. The article of claim 26 including instructions to cause the computer system to set a valid bit corresponding to a pointer in the cache when the pointer is modified by an enqueue or a dequeue operation.

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30. The article of claim 29 including instructions to cause the computer system to return to the memory pointers whose corresponding valid bits are set.

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